CLAIMS

1. A clock and data recovery circuit comprising:

- a first data input receiving a data signal of a first frequency;

- a clock defining a timing signal of a second frequency;

- a phase generator dividing a cycle of the timing signal into a number of N signal phases;

- a data sampling component sampling a portion of said data signal causing a logic output statement based on a truth table, said data sampling component comprising a buffer component for buffering said data signal and comprising a phase detector assigned to said buffer component;.

- a counter assigned to said phase detector with said logic output statement causing a reaction of said counter; and

a phase selector assigned to said counter, wherein

three or more of said clock phases are selected by said phase selector and the data sampling is triggered by said three or more clock phases.

2. A clock and data recovery circuit as claimed in claim 1, wherein

said reaction of said counter is counting up, counting down, or holding of the counter with the counter value transferred to the phase selector assigned to select the clock phases.

3. A clock and data recovery circuit as claimed in claim 1, wherein

the data signal is a binary signal having signal states zero or one defining a bit sequence.

4. A clock and data recovery circuit as claimed claim 1, wherein

said buffer component comprises bistable multivibrators.

5. A clock and data recovery circuit as claimed in claim 1, wherein

said buffer component comprises a first, a second and a third buffer portion each having a data input and a data output with the data inputs of the three buffer portions assigned to the first data input.

6. A clock and data recovery circuit as claimed in claim 5, wherein

said first, second and third buffer portions are triggered by a first clock phase i,

a second clock phase j and a third clock phase k, respectively, resulting in a buffering of the state of said data signal at said clock phases i, j and *k*.

7. A clock and data recovery circuit as claimed in claim 6, wherein the clock phases i, j and *k* are interdependent by the equations:

$j = i + N/2 - M$ *and* $k = i + N/2 + M$ if $i \leq N/2$ and

$j = I - N/2 - M$ and $k = i - N/2 + M$ if $i > N/2$

with a parameter *M* selectable within $0 < M < N/2$.

8. A clock and data recovery circuit as claimed in claim 6, further comprising a first output receiving the data signal from the buffer portion which is triggered by the clock phase i and said data signal and/or said timing signal is transmitted by said first output.

9. A clock and data recovery circuit as claimed in one of claim 5, wherein the signal states of the data signal at the data outputs of said first, second and third buffer portions are detected by said phase detector.

10. A clock and data recovery circuit as claimed in claim 9, wherein the phase detector further detects the signal state of the data signal at the clock phase i of the previous cycle of the timing signal.

11. A clock and data recovery circuit as claimed in claim 1, further comprising

a low pass filter assigned to said phase detector.

12. A clock and data recovery circuit as claimed in claim 1, further comprising

dual rail amplifiers.

13. A method for clock and data recovery comprising:

- receiving a data signal of a first frequency;
- defining a timing signal of a second frequency;
- dividing a cycle of the timing signal into a number of N signal phases;
- sampling a portion of said data signal by a data sampling component resulting in a binary number, said data sampling component comprising a buffer component buffering said data signal and comprising a phase detector;

- looking up said binary number in a truth table yielding a logic output statement; and

- transmitting said logic output statement to a counter causing a reaction of said counter wherein the phase selector selects three or more of the clock phases and triggers the data sampling by said three or more clock phases.

14. A method as claimed in claim 13, wherein

said counter is counting up, counting down, or holding the counter value as reaction on said logic output statement of the truth table transferring the counter value to the phase selector assigned to select the clock phases.

15. A method as claimed in claim 13, wherein

the data signal is a binary signal having signal states zero or one defining a bit sequence and wherein said data signal is buffered by a first, a second and a third group

of bistable multivibrators triggered by a first clock phase i, a

second clock phase *j* and a third clock phase *k*, respectively, resulting in a buffering of the state of said data signal at said clock phases i, *j* and *k*.

16. A method as claimed in claim 15, further defining the clock phases j and k by:

$-j = i + N/2 - M$ and $k = i + N/2 + M$ if $i \leq N/2$ and

$-j = i - N/2 - M$ and $k = i - N/2 + M$ *if* $i > N/2$

with selecting the parameter *M* within $0 < M < N/2$.

17. A method as claimed in claim 15 or 16, further transmitting said data signal (74) and/or said timing signal by an output with the transmission triggered by the clock phase i.

18. A method as claimed in claim 15, further detecting the state of the data signal at the clock phase i of the previous cycle of the timing signal resulting in a four digit binary number having sixteen possible values and looking up said binary number in said truth table at each cycle of the timing signal yielding said reaction of the counter.